



CTAN010: SLC vs. MLC NAND

Covered Products: All Cactus Technologies flash memory products.

1. Introduction

The development of NAND flash technology has, until recently, followed the path of traditional memory technologies, such as SRAM, DRAM, EEPROM, etc., in that each memory cell stores one bit of binary data. This type of NAND flash technology is now referred to as **Single Level Cell** or SLC.

In the push for higher densities, a new type of memory cell design that can store multiple bits of binary data per cell has been introduced recently. This type of NAND flash technology is now known as **Multi Level Cell** or MLC.

There are key differences in device characteristics and performance between SLC and MLC NAND flash. In this appnote, we will explore some of these differences.

2. MLC Has Higher Density and Lower Cost Per Bit

The current generation of MLC NAND flash device stores 2 bit per cell. This higher storage density means that for the same amount of storage, the memory array size for MLC devices is smaller than that for SLC devices. The smaller array size translates to smaller die size and, thus, lower cost per bit.

The area advantage for MLC, however, is not quite 2X that of SLC. The reason for this is because MLC needs more sophisticated program and read circuitry, thus resulting in slightly larger die area consumed by these circuits.

3. MLC NAND Has Lower Device Performance

In order to store 2 bits per cell in an MLC NAND flash cell, the programming circuitry must be able to place 4 precise quantities of charge on the floating gate of the device, using pretty much the same voltage threshold window as an SLC device. Fig. 1 shows the resulting V_t distribution for SLC vs. MLC.

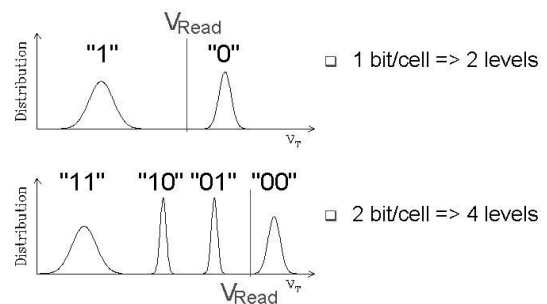


Fig. 1 SLC vs MLC V_t distribution

To achieve this precise distribution of charge on the floating gate of the flash device requires a more sophisticated and time consuming programming algorithm. As a result, the programming time for MLC NAND flash is up to 4X slower than that for SLC NAND flash.

A similar performance penalty exist for read operations because it takes a longer time for the read sensing circuitry to be able to distinguish between the four states accurately. Thus, the read access time for MLC NAND flash is up to 3X slower than that for SLC NAND flash.

4. MLC NAND Has Lower System Performance

Besides the fundamental device level performance deficiencies described above, MLC NAND also suffers from lower system level performance due to lack of support for a couple of system features: copyback programming and partial programming.

Copyback programming allows the user to move a page of data from one location in the flash device to another location without having to transfer the data in and out of the memory. For a typical 2KByte/page NAND flash device, this results in a time savings of over 170us per page. Copyback programming is most effective for wear leveling and read/modify/write operations.

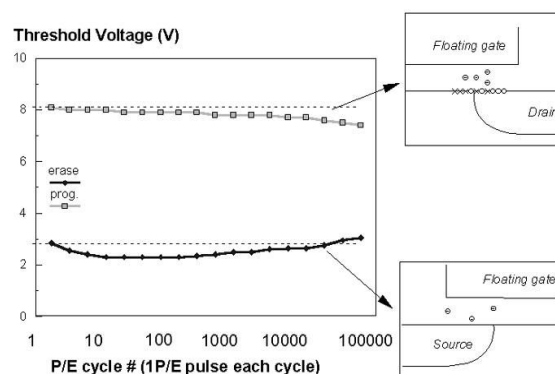
Partial programming allows the user to program only part of a page of data in the device. For a typical 2KByte/page NAND flash in a typical PC application, a page of data holds 4 sectors of data. Partial programming allows the user to program one sector's worth of data at a time. This is particularly useful for read/modify/write operations or for small block transfers.

MLC NAND, due to its particular architecture and device characteristics, is more sensitive to array disturbance phenomenon. Access to part of the array can cause disturbance to other parts of the same array. Consequently, MLC NAND manufacturers have chosen not to allow partial programming or copyback programming in order to minimize the possibility of array disturbance. The lack of these two features mean that MLC NAND is slower when the user needs to move data from one location of the device to another location. It also means that MLC NAND performance in small block operations is substantially worse than SLC NAND.

5. MLC NAND Has Lower Endurance

The process of programming a NAND flash cell results in physical damage to the thin oxide layer that separates the floating gate from the substrate.

This damage accumulates over use and the net result is that, as the number of program/erase cycles increases, the voltage threshold window that separates the program state from an erase state narrows. If this window narrows sufficiently, it will result in read sensing error. This phenomenon is illustrated in Fig.2 for SLC NAND.



In MLC NAND, the need to accommodate 4 distinct states within pretty much the same voltage threshold window means that for each state, the available threshold window is about $\frac{1}{4}$ the size as compared to SLC NAND. Since the programming mechanism in MLC NAND is the same as for SLC NAND, the damage to the oxide layer during programming is the same. And since the program/erase threshold window for MLC NAND is only $\frac{1}{4}$ that of SLC NAND, this means that the effects of the program/erase window narrowing is felt much earlier for MLC NAND as compared to SLC NAND.

Currently, SLC NAND manufacturers guarantees a minimum endurance of 100,000 program/erase cycles per cell. In contrast, current MLC NAND guarantees only a maximum of 10,000 program/erase cycles per cell. This is an order of magnitude lower endurance for MLC NAND as compared to SLC NAND.

The implication of this lower endurance limit is that MLC NAND is not suitable for applications which require frequent update of data or which require high reliability over extended operating conditions.

6. MLC NAND Has Higher Error Rates

As mentioned in the previous section, the voltage threshold window per state for MLC NAND is much smaller than that of SLC NAND. As a result, MLC NAND is more susceptible to read sensing errors. These read sensing errors are the results of program/erase threshold margins narrowing or shifting due to charge leakage from the cell or from array disturbances.

These inherently higher read error rates for MLC NAND mean that at the system level, a much stronger ECC is required to protect it against read errors during normal operation.

Note also that the effects of cell leakage and voltage margin shifting are worsened for the extended voltages and temperature range environments in industrial applications. For this reason, MLC NAND is not suitable for use in industrial grade flash storage devices.

7. MLC NAND Is Usually One Generation Behind In Process Technology

As MLC NAND is a more complicated design with lower yields, the manufacturers do not want to push the latest technology for use in MLC NAND processing. Thus, it is typical that MLC NAND process is one process node behind SLC NAND. As a result, MLC NAND is not able to fully leverage the 2X density advantage over SLC NAND.

8. Summary

In the previous sections, we have explored some of the key differences between SLC NAND and MLC NAND. The important point to remember is that while MLC NAND has some advantages in terms of higher density and lower cost per bit, it suffers from low performance, low endurance and low reliability.

Cactus Technologies believes that only SLC NAND provides the superior performance, endurance and reliability required for operation in an industrial environment. Hence, Cactus Technologies uses only SLC NAND exclusively to provide our customers with the highest quality industrial grade flash storage products.

We hope that this appnote has helped our customers to better understand the key differences between SLC NAND and MLC NAND. Should any of our readers have further questions on this issue, please feel free to direct your inquiry to our Technical Support Dept. (tech@cactus-tech.com).

9. Version History

<i>Version</i>	<i>Date</i>	<i>Change</i>
1.00	February 11, 2008	Initial Version
1.01	June 3, 2008	Minor edits